Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please cancel claims 1-46. Please add new claims 47-58.

47. (new): A processing apparatus comprising:

a memory register storage device comprising a first portion and a second portion;

a processing element comprising a first execution unit and a second execution unit for reading from and writing to the memory register storage device; and

port priority control logic for resolving a write conflict occurring when the first execution unit attempts to write to both the first portion and the second portion, and the second execution unit attempts to write to the second portion,

said port priority control logic allowing the first execution unit to write to the first portion,

said port priority control logic allowing the first execution unit to write to the second portion if the first execution unit has a higher port priority than the second execution unit,

said port priority control logic allowing the second execution unit to write to the second portion if the second execution unit has a higher port priority than the first execution unit.

48. (new): The processing apparatus of claim 47 wherein the bit width of the first portion equals the bit width of the second portion.

49. (new): The processing apparatus of claim 47 wherein the port priority is programmable.

50. (new): The processing apparatus of claim 47 wherein the memory register storage device is a computer register file.

51. (new): The processing apparatus of claim 47 wherein the processing elements reading a very long instruction word (VLIW) to determine whether to write to the first or second portion.

52. (new): The processing apparatus of claim 47 wherein the processing element further comprises a third execution unit, the third execution unit completing a write operation to the memory register storage device while conflicting write operations are prioritized for completion.

53. (new): A method for resolving write conflicts between a first execution unit and a second execution unit disposed in a processing element, the method comprising:

providing a memory register storage device comprising a first portion and a second portion;

assigning a first port priority to the first execution unit;

assigning a second port priority to the second execution unit; and

resolving a write conflict occurring when the first execution unit attempts to write to both the first portion and the second portion, and the second execution unit attempts to write to the second portion, the resolving step further comprises

allowing the first execution unit to write to the first portion,

allowing the first execution unit to write to the second portion if the first execution unit has a higher port priority than the second execution unit,

allowing the second execution unit to write to the second portion if the second execution unit has a higher port priority than the first execution unit.

54. (new): The method of claim 53 wherein the bit width of the first portion equals the bit width of the second portion.

55. (new): The method of claim 53 wherein the first port priority is programmable.

56. (new): The method of claim 53 wherein the memory register storage device is a computer register file.

57. (new): The method of claim 53 wherein the resolving step further comprises reading a very long instruction word (VLIW) to determine whether to write to the first or second portion.

58. (new): The method of claim 53 wherein the processing element further comprises a third execution unit, the method further comprising completing a write operation to the memory register storage device while conflicting write operations are prioritized for completion.